



# TG16C552

Dual UART with 16-Byte FIFO  
and Printer Port

## Features

- IBM PC/AT™ and PS/2™ compatible Dual UART
- 16-byte transmit-receive FIFO
- Four Selectable receive trigger levels
- Programmable baud rate generator
- Modem control signals
- 3.3V or 5V Operation
- Advanced Cmos Technology for Low Power
- 5, 6, 7, 8 Bit characters selection
- Even, Odd, No parity, or Force parity generations
- Status report capability
- Compatible with industry standard 16C550 UART
- CENTRONICS™ Printer Bi-directional interface
- Hardware and Software compatible with 16C452
- On-Chip Power-On-Reset function

## Applications

- High speed modems
- Serial printers
- Monitoring equipment
- Add on I/O cards
- Serial networking
- Print server
- Network Hubs and Routers
- POS Systems
- ISDN Products
- PC-104/104+ Cards
- Embedded Systems
- PCI/Compact PCI Interface Cards

## Ordering Information

Part Number	Package	Temperature
TG16C552CJ	68-Pin PLCC	0° C to 70° C
TG16C552IJ	68-Pin PLCC	-40° C to +85° C

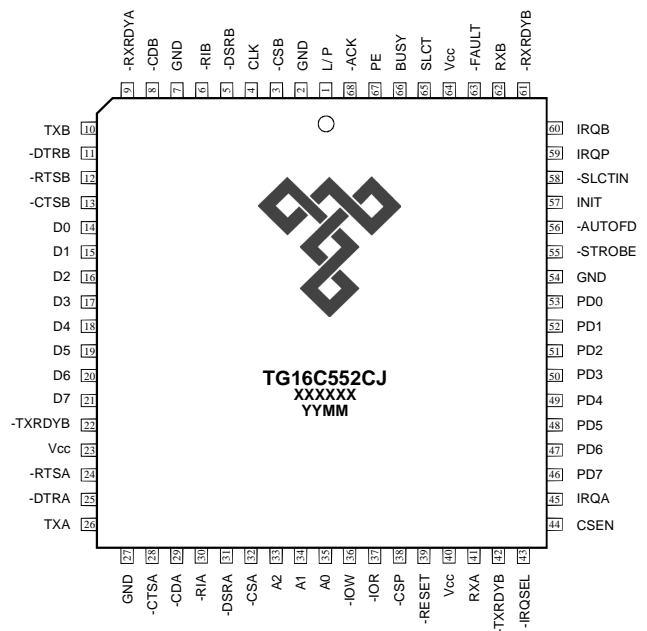
The C temperature product will operate over the Industrial Temperature range (-40°C to +85°C). Contact Factory for 100% testing of Industrial Temperature ranges.

## General Description

The TG16C552 is a dual-channel high performance UART offering data rates up to 1.5 Mbps. The TG16C552 is a dual functional upgrade of the industry standard 16C450 with the addition of a 16-byte transmit and receive FIFO. The TG16C552 performs serial-to-parallel conversions on data received from a peripheral device or modem and parallel-to-serial conversion on data received from its CPU. In addition, the TG16C552 provides the user with a fully bi-directional parallel data port that supports standard CENTRONICS™ interface with PS/2™ bi-directional option.

The TG16C552 is ideally suited for PC and embedded systems applications, such as high speed COM ports or internal modems. The TG16C552 is available in 68 pin PLCC package, It is fabricated in an advanced 0.5µ CMOS process to achieve low power drain and high-speed performance.

## 68 Pin Plastic PLCC Package

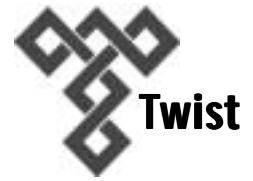


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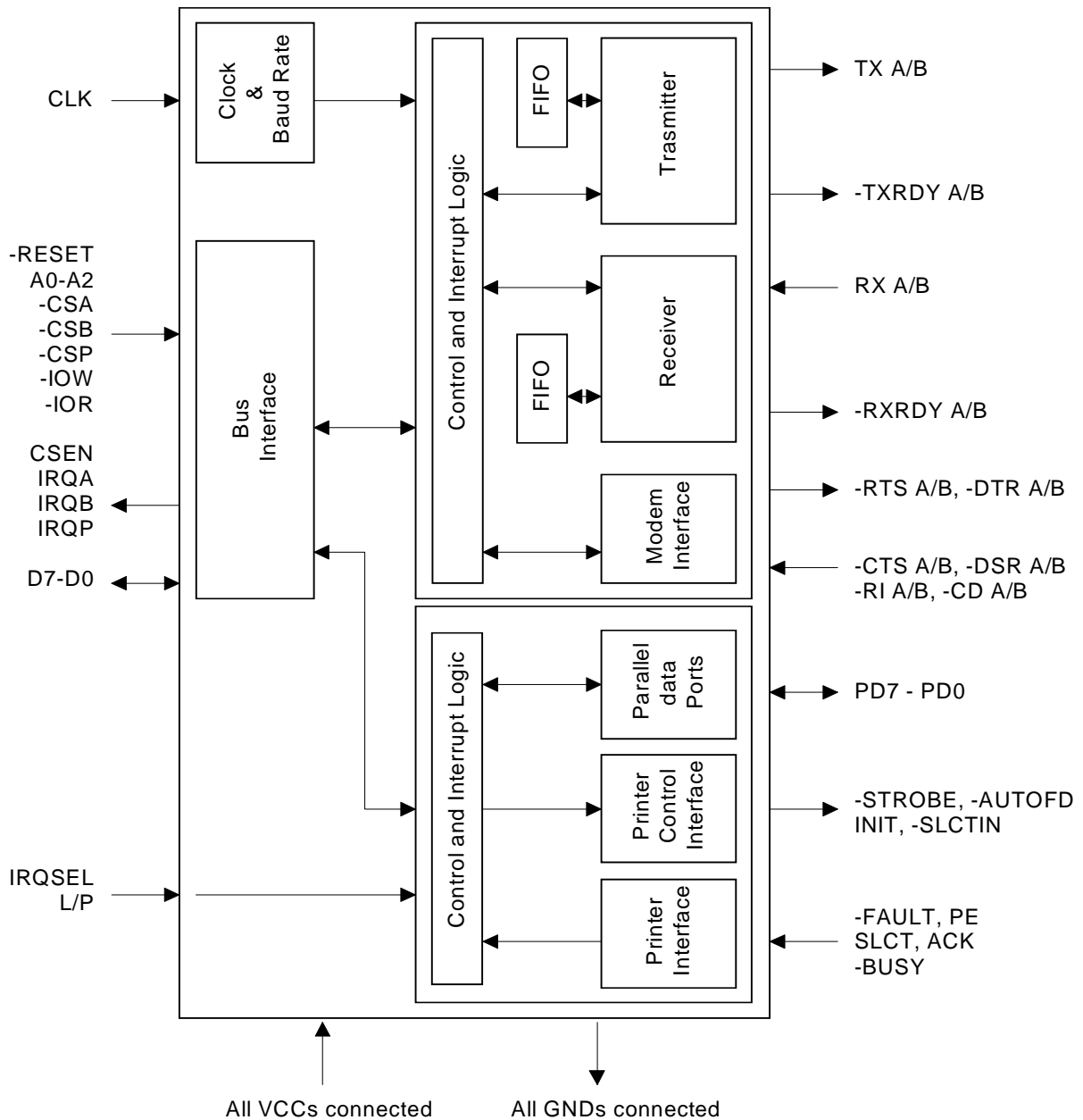
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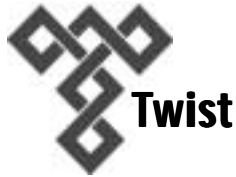
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TG16C552 Block Diagram





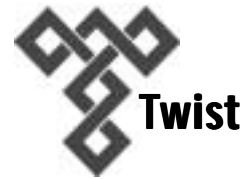
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## Dual UART with 16-Byte FIFO and Printer Port

Pin name	68	Type	Description
L/P	1	I	Standard or PS/2™ parallel port select (internal pull-up). When this pin is left open or pulled high, bi-directional parallel port is selected (Latched mode). Standard Centronics parallel port is selected when it is pulled low or connected to GND pin (Pulsed mode). A logic 1 sets the DCR register bit-5 only.
GND	2	PWR	Supply ground (must be connected).
-CSB	3	I	Active low, UART-B chip registers selected.
CLK	4	I	External clock input pin.
-DSRB	5	I	Active low, UART-B data-set-ready signal.
-RIB	6	I	Active low, UART-B ring-detect signal.
GND	7	PWR	Supply ground (must be connected).
-CDB	8	I	Active low, UART-B Carrier-detect signal. When low this indicates that Modem or data set has detected the data carrier. -CDB has no effect on the transmitter.
-RXRDYA	9	O	Active low, UART-A receive data ready. Receive DMA signaling is available with this pin. In FIFO mode, one of two types of DMA signaling can be selected using FCR bit-3. DMA mode [0]: (FCR bit-3=0) supports single transfer DMA (16C450 mode) in which a transfer is made between CPU bus cycle. -RXRDYA pin will be low active when there is at least one character in receive holding register or FIFO. -RXRDYA pin will be inactive (high) when there are no more characters in the FIFO or holding register. DMA mode [1]: (FCR bit-3=1) supports multi transfer DMA in which multiple transfers are made continuously until the receive FIFO has been emptied. -RXRDYA pin will be low active when trigger level or the time-out has been reached.
TXB	10	O	UART-B Serial data output. During reset, this pin is a logic 1.
-DTRB	11	O	Active low, UART-B data-terminal-ready signal. It is set to high (inactive) after a hardware reset or during internal loop-back mode. When low, this output indicates to the Modem or data set that the UART-B is ready to establish a communication link. -DTRB has no effect on the transmitter or receiver. Writing a 1 to MCR bit-0, sets -DTR to a 0. This pin is a logic 1 after writing 0 to MCR bit-0 or a reset condition.
-RTSB	12	O	Active low, UART-B request-to-send signal. It is set to high (inactive) after a hardware reset or during internal loop-back mode. When low, this indicates that Modem or data set is ready to establish a communication link. -RTSB has no effect on the transmitter or receiver.
-CTSB	13	I	Active low, UART-B clear-to-send signal. When low this indicates that Modem or data set is ready to exchange data. -CTSB has no effect on the transmitter. This pin can be tested by reading MSR bit-4.
D0	14	I/O	Data bus. Eight data lines with tri-state outputs provided as a bi-directional path for data. This pin is the least significant bit of the data bus and the first data bit in a transmit or receive serial data stream.

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Pin name	68	Type	Description
D1	15	I/O	Data bus bit-1. See D0 description.
D2	16	I/O	Data bus bit-2. See D0 description.
D3	17	I/O	Data bus bit-3. See D0 description.
D4	18	I/O	Data bus bit-4. See D0 description.
D5	19	I/O	Data bus bit-5. See D0 description.
D6	20	I/O	Data bus bit-6. See D0 description.
D7	21	I/O	Data bus bit-7. Most significant bit of the data bus. See D0 description.
-TXRDYA	22	O	Active low, UART-A transmitter ready. Transmit DMA signaling is available with this pin. In FIFO mode, one of two types of DMA signaling can be selected using FCR bit-3. DMA mode [0]: (FCR bit-3=0) supports single transfer DMA in which a transfer is made between CPU bus cycle. -TXRDYA pin will be low (active) when there are no characters in the transmit FIFO, transmit holding register. DMA mode [1]: (FCR bit-3=1) supports multi transfer DMA in which multiple transfers are made continuously until transmit FIFO has been filled. This pin will become inactive (high) when transmit FIFO is completely full.
VCC	23	PWR	Supply voltage. 3.3V to 5V (must be connected).
-RTSA	24	O	Active low, UART-A request-to-send signal. It is set to high (inactive) after a hardware reset or during internal loop-back mode. When low, this indicates that Modem or data set is ready to establish a communication link. -RTSA has no effect on the transmitter or receiver.
-DTRA	25	O	Active low, UART-A data-terminal-ready signal. It is set to high (inactive) after a hardware reset or during internal loop-back mode. When low, this output indicates to the Modem or data set that the UART-A is ready to establish a communication link. -DTRA has no effect on the transmitter or receiver.
TXA	26	O	UART-A Serial data output. This pin is 1 during a reset.
GND	27	PWR	Supply ground (must be connected).
-CTSA	28	I	Active low, UART-A clear-to-send signal. When low this indicates that Modem or data set is ready to exchange data. This pin can be tested by reading MSR bit-4. -CTSA has no effect on the transmitter.
-CDA	29	I	Active low, UART-A Carrier-detect signal. When low this indicates that Modem or data set has detected the data carrier. -CDA has no effect on the transmitter.
-RIA	30	I	Active low, UART-A ring-detect signal.
-DSRA	31	I	Active low, UART-A data-set-ready signal.
-CSA	32	I	Active low, UART-A chip registers selected.



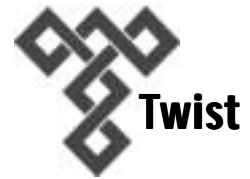
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Pin name	68	Type	Description
A2	33	I	See A0.
A1	34	I	See A0.
A0	35	I	Register select address line. These address lines from the CPU determine which internal register is accessed.
-IOW	36	I	Active low I/O Write input. CPU is allowed to write data into a selected register. The data write operation, depends upon chip selects (CSA, CSB, CSP) and A0-2 address lines.
-IOR	37	I	Active low I/O Read input. Enables selected register to output data to D0-7 bus. The data output depends upon chip selects (CSA, CSB, CSP) and A0-2 address lines.
-CSP	38	I	Active low, Parallel printer port chip registers selected.
-RESET	39	I	Active low hardware reset. Resets all internal registers to known values. See Power-On-Reset for further description of this function.
VCC	40	PWR	Supply voltage, 3.3V to 5V (must be connected).
RXA	41	I	UART-A, Serial data input. This pin is a logic 1 during reset.
-TXRDYB	42	O	See -TXRDYA.
-IRQSEL	43	I	Parallel port interrupt mode select (internal pull-up). Interrupt pulsed mode is selected when this pin is pulled low or connected to GND, the ACK input pin is re-directed to INTP output pin when DCR Bit-4 is set to "1". Interrupted latched mode (PS/2™) is selected when this pin is left open or pulled up to VCC. IRQP will go active on the rising edge of the -ACK input pin.
CSEN	44	O	Active high external transceiver drive disable. This pin goes high when CPU is not reading from the TG16C552 internal registers. This output can be left open if no external transceiver is used.
IRQA	45	O	UART-A, Active high interrupt output. This signal goes high (active) when an interrupt condition occurs. Interrupt out is gated with IER bit 0-3 and MCR bit-3.
PD7	46	I/O	Bi-directional Parallel port data bit-7.
PD6	47	I/O	Bi-directional Parallel port data bit-6.
PD5	48	I/O	Bi-directional Parallel port data bit-5.
PD4	49	I/O	Bi-directional Parallel port data bit-4.
PD3	50	I/O	Bi-directional Parallel port data bit-3.
PD2	51	I/O	Bi-directional Parallel port data bit-2.
PD1	52	I/O	Bi-directional Parallel port data bit-1.

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Pin name	68	Type	Description
PDO	53	I/O	Bi-directional Parallel port data bit-0.
GND	54	PWR	Supply ground (must be connected).
-STROBE	55	I/O	Printer data strobe (open drain with internal pull-up). On the rising edge of the -STROBE, data is latched into printer port.
-AUTOFD	56	I/O	Printer Auto Feed (open drain with internal pull-up). When this pin goes low, continuous form paper is to be autofed to the printer.
INIT	57	I/O	Initialize the printer (open drain with internal pull-up). When this pin goes low, printer starts it's initialization routine.
-SLCTIN	58	I/O	Printer select (open drain internal pull-up). Selects the printer when it is active (low).
IRQP	59	O	Printer port interrupt. IRQP is an active-high, three state output generated by the positive transition of ACK. It is enabled by DCR bit-4. This pin is also controlled by IRQSEL pin. After reset, IRQP is set to three state mode.
IRQB	60	O	UART-B, Active high interrupt output. This signal goes high (active) when an interrupt condition occurs. Interrupt out is gated with IER bit 0-3 and MCR bit-3.
-TXRDYB	61	O	Active low, UART-B transmitter ready. Transmit DMA signaling is available with this pin. In FIFO mode, one of two types of DMA signaling can be selected using FCR bit-3. DMA mode [0]: (FCR bit-3=0) supports single transfer DMA in which a transfer is made between CPU bus cycle. -TXRDYB pin will be low (active) when there are no characters in the transmit FIFO, transmit holding register. DMA mode [1]: (FCR bit-3=1) supports multi transfer DMA in which multiple transfers are made continuously until transmit FIFO has been filled. This pin will become inactive (high) when transmit FIFO is completely full.
RXB	62	I	UART-B, Serial data input. This pin is a logic 1 during reset.
-FAULT	63	I	Line printer error. Printer reports an error by holding this line low during the error condition.
VCC	64	PWR	Supply voltage, 3.3V to 5V (must be connected).
SLCT	65	I	Printer selected. SLCT goes high, when printer has been selected.
-BUSY	66	I	Printer busy. -BUSY goes high, when printer is not ready to accept data.
PE	67	I	Printer paper empty. PE goes high when printer is out of paper.
-ACK	68	I	Printer acknowledge. ACK goes low to indicate a successful data transfer has taken place. It generates a printer port interrupt during its positive transition.



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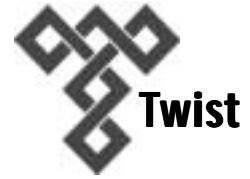
## Internal Registers

A2	A1	A0	READ MODE	WRITE MODE
			<b>Uart Registers</b>	
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Identification Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
			<b>Parallel Port Registers</b>	
0	0	0	Printer Input Data Register	Printer Output data Register
0	0	1	Device Status Register	
0	1	0	Device Command Register	Device Control Register

Divisor Latch registers are only accessible when Line Control Register (LCR) bit-7 is set to a logic 1.

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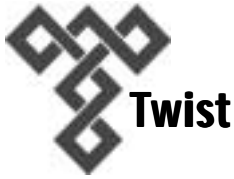
**Internal Registers Table**

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
<b>Uart Registers (1)</b>											
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0	1	0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	0	IIR	FIFO enabled	FIFO enabled	0	0	INT priority bit-2	INT priority bit-1	INT priority bit-0	INT status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0	loop back	IRQA/B enable (OP2)	(OP1)	RTS	DTR
1	0	1	LSR	FIFO Recv error	transmit empty	transmit holding empty	Break interrupt	Framing error	Parity error	Overrun error	Receive data ready
1	1	0	MSR	CD	RI	DSR	CTS	delta -CD	delta -RI	delta -DSR	delta -CTS
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL (2)	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM (2)	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
<b>Parallel Port Registers (3)</b>											
0	0	0	PD	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DSR	-BUSY	ACK	PE	SLCT	-FAULT	IRQR	1	1
0	1	0	DCR	0	0	DIR PD 0-7	IRQ Enable	-SLCTIN	INIT	-AUTOFD	-STROBE

(1) Only accessible when CSA or CSB = 0.

(2) DLL and DLM are accessible only when LCR Bit-7=1.

(3) Only accessible when -CSP = 0, dependant on the levels of L/P and DCR bit-5 or IOSEL register.



### UART OPERATION

#### Transmitter Holding Register (THR)

The UART transmitter section of the TG16C552 consists of a transmitter holding register (THR) and a transmitter shift register (TSR). The THR is actually a 16-byte FIFO. Transmitter section control is a function of the UART line control register. The UART THR receives data off the internal data bus and when the shift register is idle, moves it into the TSR. The TSR serializes the data and outputs it at TX. In the 16C450 mode, if the THR is empty and the transmitter holding register empty (THRE) interrupt is enabled (IER-1=1), an interrupt is generated. This interrupt is cleared when a character is loaded into the register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

#### Receive Holding Register (RHR)

The UART receiver section of the TG16C552 consists of a receiver shift register (RSR) and a receiver holding register (RHR). The RHR is actually a 16-byte FIFO. Timing to receive holding register is supplied by the 16x-receiver clock (RCLK). Receiver section control is a function of the UART line control register.

The UART RHR receives serial data from RX. The RSR then concatenates the data and moves it into the RHR FIFO. In the 16C450 mode, when a character is placed in the receiver holding register and the received data available interrupt is enabled (IER-0=1), an interrupt is generated. This interrupt is cleared when the data is read out of the receiver holding register. In the FIFO mode, the interrupts are generated based on the control setup in the FIFO control register.

#### Interrupt Enable Register (IER)

The interrupt enables register enables each of the five types of interrupts and INT pin response to an interrupt generation. The interrupt enable register can also be used to disable the interrupt system by setting bits 0-3 to logic 0. The contents of this register are described below.

##### IER Bit-0:

0 = Disable the received data available interrupt.  
1 = Enables the received data available interrupt.

##### IER Bit-1:

0 = Disable the transmitter holding register empty interrupt.  
1 = Enable the transmitter holding register empty interrupt.

##### IER Bit-2:

0 = Disables the receiver line status interrupt.  
1 = Enables the receiver line status interrupt.

##### IER Bit-3:

0 = Disables the modem status interrupt.  
1 = Enables the modem status interrupt.

##### IER Bits 4-7:

These bits are not used (always set to 0).

#### Interrupt Identification Register (IIR)

The UART has an on chip interrupt generation and prioritization capability that permits a flexible interface with most popular microprocessors.

##### IIR Bit-0:

0 = An interrupt is pending. Used either in a hardware prioritized or polled interrupt system.  
1 = No interrupt is pending.

##### IIR Bits 1-2:

The UART provides four prioritized levels of interrupts:

- Priority 1 - Receiver line status (highest priority) (LSR)
- Priority 2 - Receiver data ready (RXRDY)
- Priority 2 - Receiver character time-out (RXRDY)
- Priority 3 - Transmitter holding register empty (TXRDY)
- Priority 4 - Modem status (lowest priority) (MSR)

When an interrupt is generated, the interrupt identification register indicates that an interrupt is pending and encodes the type of interrupt in its three least significant bits (bits 0, 1, and 2).

#### Interrupt Priority decode

Bit-3	Bit-2	Bit-1	Bit-0	Interrupt source
0	1	1	0	Receive line status register
0	1	0	0	Receive data ready
1	1	0	0	Receive time-out
0	0	1	0	Transmit holding empty
0	0	0	0	Modem status register

The bits are used to identify the highest priority interrupt pending.

##### IIR Bit-3:

0 = In the 16C450 mode. In FIFO mode, this bit is set along with bit-2 to indicate that a time-out interrupt is pending.

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### IIR Bits 4-5:

These bits are not used (always reset at 0).

### IIR Bits 6-7:

0 = In the 16C450 mode.  
1 = When FCR-0 is equal to 1.

### FIFO control register (FCR)

The FIFO control register (FCR) is a write only register. The (FCR) enables and clears the FIFO, sets the receiver FIFO trigger level, and selects the type of DMA signaling.

### FCR Bit-0:

0 = 16C450 mode, disables the transmitter and receiver FIFO.  
1 = Enables the transmitter and receiver FIFO. This bit must be set to 1 when other (FCR) bits are written to or they are not programmed. Changing this bit clears the FIFO.

### FCR Bit-1:

0 = Normal operation  
1 = Clears all bytes in the receiver FIFO and resets its counter logic to 0. The shift register is not cleared. The one that is written to this bit position is self-clearing.

### FCR Bit-2:

0 = Normal operation  
1 = Clears all bytes in the transmit FIFO and resets its counter logic to 0. The shift register is not cleared. The one that is written to this bit position is self-clearing.

### FCR Bit-3:

0 = Mode [0]:  
Supports single transfer DMA (16C450 mode) in which a transfer is made between CPU bus cycle.

### -RXRDY Pin:

Will be active low when there is at least one character in receive holding register or FIFO. -RXRDY pin will be inactive (high) when there are no more characters in the FIFO or holding register. This pin will also be active low when trigger level or the time-out has been reached. Supports multi-transfer DMA in which multiple transfers are made continuously until transmit FIFO has been filled. This pin will become inactive (high) when transmit FIFO is completely full or reached trigger level.

### -TXRDY Pin:

This pin will be active low until transmit FIFO has been filled. This pin will become inactive (high) when transmit FIFO is completely full. It will also be active low when no characters are in the transmit FIFO, transmit holding register.

1 = Mode [1]:

Supports multi transfer DMA in which multiple transfers are made continuously until the receive FIFO has been emptied.

### FCR its 4-5:

These bits are not used.

### FCR Bits 6-7:

These bits are used to set the trigger level for the receiver FIFO interrupt.

### Receive trigger levels (BYTES)

Bit-7	Bit-6	RX FIFO trigger level
0	0	1
0	1	4
1	0	8
1	1	14

### Line Control Register (LCR)

The system programmer controls the format of the asynchronous data communication exchange through the line control register. In addition, the programmer is able to retrieve, inspect, and modify the contents of the line control register; this eliminates the need for separate storage of the line characteristics in system memory.

### LCR Bits 0-1:

These two bits specify the number of bits in each transmitted or received serial character.

### Word Length

Bit-1	Bit-0	Word length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

### LCR Bit-2:

This bit specifies, 1, 1-1/2, or 2 stop bits in each transmitted character. When bit-2 is reset to 0, one stop bit is generated in the data. When bit-2 is set to 1, the number of stop bits generated is dependent on the word length selected with bits 0 and 1. The receiver clocks only the first stop bit regardless of the number of stop bits selected. The number of stop bits generated in relation to word length and bit-2.



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### Stop Bits

Bit-2	Word length	Stop bit(s)
0	X	1
1	5 bits	1-1/2
1	6 bits	2
1	7 bits	2
1	8 bits	2

### LCR Bit-3:

0 = Parity is disabled. No parity is generated or checked.  
 1 = Parity bit is generated in transmitted data between the last data word bit and the first stop bit. In received data, parity is checked.

### LCR Bit-4:

0 = ODD parity select bit. When parity is enabled by bit-3, a 1 in bit-4 produces odd parity (an odd number of 1's in the data and parity bits).  
 1 = Even parity select bit. When parity is enabled by bit-3, a 1 in bit-4 produces even parity (an even number of 1's in the data and parity bits).

### LCR Bit-5:

0 = Stick parity is disabled.  
 1 = Stick parity bit. When bits 3-5 are set to 1 the parity bit is transmitted and checked as a 0. When bits-3 and 5 are 1's and bit-4 is a 0, the parity bit is transmitted and checked as 1.

### LCR Parity selection

Bit-5	Bit-4	Bit-3	Parity type
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Forced parity "1"
1	1	1	Forced parity "0"

### LCR Bit-6:

0 = Normal operation. Break condition is disabled and has no effect on the transmitter logic.  
 1 = Force a break condition. A condition where TX is forced to the space (low) state.

### LCR Bit-7:

0 = Normal operation.  
 1 = Divisor latch enable. Must be set to 1 to access the divisor latches of the baud generator during a read or write. Bit-7 must be reset to 0 during a read or write to the receiver holding, the transmitter holding register, or the interrupt enable register.

### Modem Control Register (MCR)

The modem control register is an 8-bit register that controls an interface with a modem, data set, or peripheral device that is emulating a modem.

### MCR Bit-0:

0 = Sets the -DTR output pin to high.  
 1 = Sets the -DTR output pin to low.

### MCR Bit-1:

0 = Sets the -RTS output pin to high.  
 1 = Sets the -RTS output pin to low.

### MCR Bit-2:

0 = Sets the -OP1 to high during loop-back mode.  
 1 = Sets the -OP1 to low during loop-back mode.

### MCR Bit-3:

0 = Sets IRQ output pin to three state. Sets the -OP2 to high during loop-back mode.  
 1 = Sets IRQ output pin to active mode. Sets the -OP2 to low during loop-back mode.

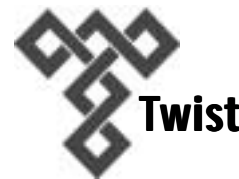
### MCR Bit-4:

0 = Normal operation.  
 1 = Internal loop back mode. Provides a local loop-back feature for diagnostic testing of the UART. When LOOP is set to 1, the following occurs:

The transmitter TX pin is set to high.  
 The receiver RX pin is disconnected.  
 The output of the transmitter shift register is looped back into the receiver shift register input.  
 The four modem inputs (-CTS, -DSR -CD and -RI) pins are disconnected. The four modem outputs (-DTR, -RTS, -OP1, and -OP2) pins are internally connected to the four modem inputs. The four modem outputs are forced to the high levels.

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## Dual UART with 16-byte FIFO and Printer Port



In the diagnostic mode, data that is transmitted is immediately received. This allows the processor to verify transmit and receive data paths to the UART. The receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the modem control interrupt sources are now the lower four bits of the modem control register instead of the four modem control inputs. All interrupts are still controlled by the interrupt enable register.

### **MCR bits 5-7:**

These bits are not used.

### **Line Status Register (LSR)**

The line status register provides information to the CPU concerning the status of data transfers. The line status register is intended for read operations only; writing to this register is not recommended. Bits 1-4 are the error conditions that produce a receiver line status interrupt.

#### **LSR Bit-0:**

0 = No data in receive holding or FIFO.

1 = Data ready indicator for the receiver. This bit is set to 1 whenever a complete incoming character has been received and transferred into the receiver holding register or the FIFO. It is reset to 0 by reading all of the data in the receiver holding register or the FIFO.

#### **LSR Bit-1:**

0 = Normal operation. No overrun error.

1 = It indicates that before the character in the receiver holding register was read, it was over written by the next character transferred into the register. OE is reset every time the CPU reads the contents of the line status register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

#### **LSR Bit-2:**

0 = Normal operation. No parity error.

1 = It indicates that the parity of the received data character does not match the parity selected in the line control register. PE is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO.

#### **LSR Bit-3:**

0 = Normal operation. No framing error.

1 = It indicates that the received character did not have a valid stop bit. FE is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. The UART tries to re-synchronize after a framing error. To accomplish this, it is assumed that the framing error is due to the next start bit.

#### **LSR Bit-4:**

0 = Normal operation.

1 = It indicates that the received data input was held in the logic low state for longer than a full word transmission time. A full word transmission time is defined as the total time to transmit the start, data, parity, and stop bits. BI is reset every time the CPU reads the contents of the line status register. In the FIFO mode, this error is associated with the particular character in the FIFO to which it applies. This error is revealed to the CPU when its associated character is at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO.

#### **LSR Bit-5:**

0 = At least one byte is written to the transmit FIFO or transmit holding register.

1 = Transmitter holding register is empty, indicating that the UART is ready to accept a new character. If the THRE interrupt is enabled when THRE is set to 1, an interrupt is generated. THRE is set to 1 when the contents of the transmitter holding register are transferred to the transmitter shift register.

#### **LSR Bit-6:**

0 = When either the transmitter holding register or the transmitter shift register contains a data character.

1 = Transmitter holding register and the transmitter shift register are both empty.

#### **LSR Bit-7:**

0 = In the 16C450, this bit is always reset to 0.

1 = In the FIFO mode, at least one parity, framing, or break error in the FIFO. It is cleared when the microprocessor reads the LSR and there are no subsequent errors in the FIFO.



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## Dual UART with 16-Byte FIFO and Printer Port

### Modem Status Register (MSR)

The modem status register is an 8-bit register that provides information about the current state of the control lines from the modem, data set, or peripheral device to the CPU. Additionally, four bits of this register provide change information, when input from the modem changes state, the appropriate bit is set to 1. All four bits are reset to 0 when the CPU reads the modem status register.

#### MSR Bit-0:

0 = No change to -CTS input.

1 = Indicates that the -CTS input has changed state since the last time it was read by the CPU. When interrupt is enabled, a modem status interrupt is generated.

#### MSR Bit-1:

0 = No change to -DSR input.

1 = Indicates that the -DSR input has changed state since the last time it was read by the CPU. When interrupt is enabled, a modem status interrupt is generated.

#### MSR Bit-2:

0 = No change to -RI input.

1 = Indicates that the -RI input has changed from a low to a high level. When -RI is set to 1 and the modem status interrupt is enabled, a modem status interrupt is generated.

#### MSR Bit-3:

0 = No change to -CD input.

1 = Indicates that the -CD input has changed state since the last time it was read by the CPU. When interrupt is enabled, a modem status interrupt is generated.

#### MSR Bit-4:

Complement of the clear to send (-CTS) input. When the UART is in the diagnostic test mode it is equal to -RTS.

#### MSR Bit-5:

Complement of the data set ready (-DSR) input. When the UART is in the diagnostic test mode it is equal to -DTR.

#### MSR Bit-6:

Complement of the ring indicator (-RI) input. When the UART is in the diagnostic test mode it is equal to -OP1.

#### MSR Bit-7:

Complement of the data carrier detect (-CD) input. When the UART is in the diagnostic test mode it is equal to -OP2.

### Scratch Pad Register (SPR)

The scratch pad register is an 8-bit register that is intended for programmer use as a scratch-pad in the sense that it temporarily holds the programmer data without affecting any other UART operation.

### Programmable Baud-Rate Generator

The UART contains a programmable baud generator that takes a clock input in the range between 1 MHz and 24 MHz and divides it by a divisor in the range between 1 and  $(2^{16}-1)$ . The output frequency of the baud generator is 16 times the baud rate. Two 8-bit registers, called divisor latches, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the UART in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded to prevent long counts on initial load.

#### Baud rate generator programming table @ 1.8432 MHz

Baud Out	DLM (hex)	DLL (hex)
115.2k	00	01
57.6k	00	02
38.4k	00	03
19.2	00	06
9600	00	0C
2400	00	30
1200	00	60
600	00	C0
300	01	80
150	03	00
50	09	00

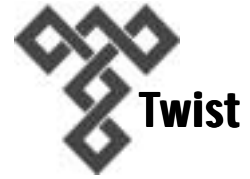
### FIFO interrupt mode operation

When the receiver FIFO and receiver interrupts are enabled (FCR-0=1, IER-0=1, IER-2=1), a receiver interrupt occurs as follows:

The received data available interrupt issued to the microprocessor when the FIFO has reached its programmed trigger level. It is cleared when the FIFO drops below its programmed trigger level. The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.

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## Dual UART with 16-byte FIFO and Printer Port



The receiver line status interrupt has higher priority than the received data available interrupt. The data ready bit (LSR-0) is set when a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

When the receiver FIFO and receiver interrupts are enabled, FIFO time-out interrupt occurs when the following conditions exist:

At least one character is in the FIFO.

The most recent serial character was received more than four continuous character times ago (if two stop bits are programmed, the second one is included in this time delay).

The most recent microprocessor read of the FIFO occurred more than five continuous character times ago. When a time-out interrupt has occurred, it is cleared and the timer is reset when the microprocessor reads one character from the receiver FIFO.

When a time-out interrupt has not occurred, the time-out timer is reset after a new character is received or after the microprocessor reads the receiver FIFO.

When the transmitter FIFO and THRE interrupt are enabled (FCR-0=1, IER-1=1), transmit interrupts occur as follows:

The occurrence of transmitter holding register empty interrupt is delayed one character time minus the last stop bit time when there have not been at least two bytes in the transmitter FIFO at the same time since the last time the transmitter FIFO was empty. It is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to transmit FIFO while servicing this interrupt) or the IIR is read. The first transmitter interrupt after changing FCR is immediate if it is enabled.

The transmitter empty indicator is delayed one character time when there has not been at least two bytes in the transmitter FIFO at the same time since the last time that TEMT=1. TEMT is set after the stop bit has been completely shifted out.

The transmitter FIFO empty indicator works the normal way in this mode and is not delayed. Character time-out and receiver FIFO trigger-level interrupts have the same priority as the current received data available interrupt.

## PARALLEL PORT OPERATION

### Data Register

Data register is cleared at initialization by -RESET. During a write operation, the Data register latches the contents of the data bus with the rising edge of the -LOW input. The contents of this register are buffered and output onto the PD7-0 ports. During a read operation PD7-0 ports are buffered and output to the host CPU on the falling edge of the -IOR input.

### Device Status Register

The contents of this register are latched for the duration of an -IOR cycle. The bits of the Status Port are defined as follows.

#### DSR Bit-1-0:

Not used and set to "1".

#### DSR Bit-2:

0 = ACK input pin is at low state (IRQP follows the ACK pin function), when standard CENTRONICS™ mode is selected. Normal (no interrupt) when PS/2™ mode is selected.

1 = Normal (no interrupt), standard mode operation. IRQP is active (interrupt is generated on the rising edge of the ACK). It is cleared when DSR is read.

#### DSR Bit-3:

0 = Printer reports error condition.

1 = Normal operation.

#### DSR Bit-4:

0 = Printer is off line, SLCT=0.

1 = Printer is on line, SLCT=1.

#### DSR Bit-5:

0 = Normal operation, PE=0.

1 = Paper End is detected, PE=1.

#### DSR Bit-6:

0 = State of the ACK pin (ACK = low).

1 = State of the ACK pin, inactive (ACK = high).

#### DSR Bit-7:

0 = -BUSY pin is high, printer is not ready to take data.

1 = -BUSY pin is low, printer is read to take data.



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Dual UART with 16-Byte FIFO  
and Printer Port

## Device Control Register

This register controls the printer port output logic states and the printer interrupt IRQP. The status of this register can be read by reading the **Device Command Register**. The Device Command Register's bits are the same as the Device Control Register, except bits 5-7 are not used.

### DCR Bit-0

0 = Sets the -STROBE pin to high.  
1 = Sets the -STROBE pin to low. PD7-0 data are latched into printer

### DCR Bit-1:

0 = Sets the -AUTOFD pin to high. Printer generates auto line feed after each line is printed.  
1 = Sets the -AUTOFD pin to low. No auto feed function.

### DCR Bit-2:

0 = Sets the INIT pin to high.  
1 = Sets the INIT pin to low.

### DCR Bit-3:

0 = Sets the -SLCTIN pin to high. Selects the printer.  
1 = Sets the -SLCTIN pin to low. Printer is not selected.

### DCR Bit-4:

0 = IRQP pin is set to three state mode. ACK pin has no effect on the IRQP pin.  
1 = Activates the IRQP pin. The IRQP follows the ACK input pin during standard mode, latches high on the rising edge of the ACK, when PS/2™ mode is selected.

### DCR Bit-5:

0 = PD7-0 pins are in the output mode.  
1 = PD7-0 pins are in the input mode.  
For these conditions, the L/P pin must be equal to 1.

### DCR Bits 7-6:

Not used, set to "0".

### Input/Output Select:

This bit (IOSEL) along with the state of L/P sets the direction of PD7-0. This register is only used when L/P=0.  
Logic 55 (hex) and L/P=0: PD7-0 are in the input mode.  
Logic AA (hex) and L/P=0: PD7-0 are in the output mode.

## Power-On-Reset.

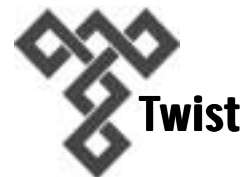
The TG16C554 has a built in POR function. This function allows the -RESET pin to be permanently tied high. Upon power-on, a 2μs reset pulse is internally generated to reset the device. If this pin is not tied high, a 2μs reset pulse is created if the incoming reset pulse is less than 2μs in duration.

## Master reset conditions

Register	Bits	State
IER	Bit 7-0	0
FCR	Bit 7-0	0
IIR	Bit 0	1
IIR	Bit 7-1	0
LCR	Bit 7-0	0
MCR	Bit 7-0	0
LSR	Bit 4-0	0
LSR	Bit 6-5	1
LSR	Bit 7	0
MSR	Bit 3-0	0
SPR	Bit 7-0	AA
DLL	Bit 0	1
DLL	Bit 7-1	0
DLM	Bit 7-0	0
DPORT	Bit 7-0	0
DSR	Bit 2-0	1
DCR	Bit 1-0	0
	Bit 3-2	1
	Bit 7-4	0

# TG16C552

Dual UART with 16-byte FIFO  
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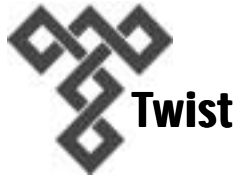
## Absolute Maximum Ratings

Supply Range	6 Volts
Voltage at any pin	GND – 0.3 to VCC +0.3
Operating Temperature	-40° C to 85° C
Storage Temperature	-65° C to 150° C
Package Dissipation	1000 mW
ESD	±2000 Volts
Latch up	220 mA

## DC Electrical Specifications

T = 0° C to 70° C (T = -40° C to +85° C for industrial tested "I" grade parts), VCC = 3.3V to 5V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3V		Limits 5V		Unit	Condition
		Min	Max	Min	Max		
Viclk	Clock input low level	-0.3	0.6	-0.5	0.6	V	External clock
Vihck	Clock input high level	2.0	VCC	2.0	VCC	V	External clock
Vil	Input low level	-0.3	0.8	-0.5	0.8	V	
Vih	Input high level	2.0	VCC	2.4	VCC	V	
Vol	Output low level				0.4	V	Iol = 6 mA
Vol	Output low level		0.4			V	Iol = 4 mA
Voh	Output high level			2.4		V	Ioh = -6 mA
Voh	Output high level	2.0				V	Ioh = -4 mA
Iil	Input leakage current		±10		±10	µA	
Icc	Operating current		2		3	mA	
Cp	Input pin Capacitance		5		5	pF	



# TG16C552

Dual UART with 16-Byte FIFO  
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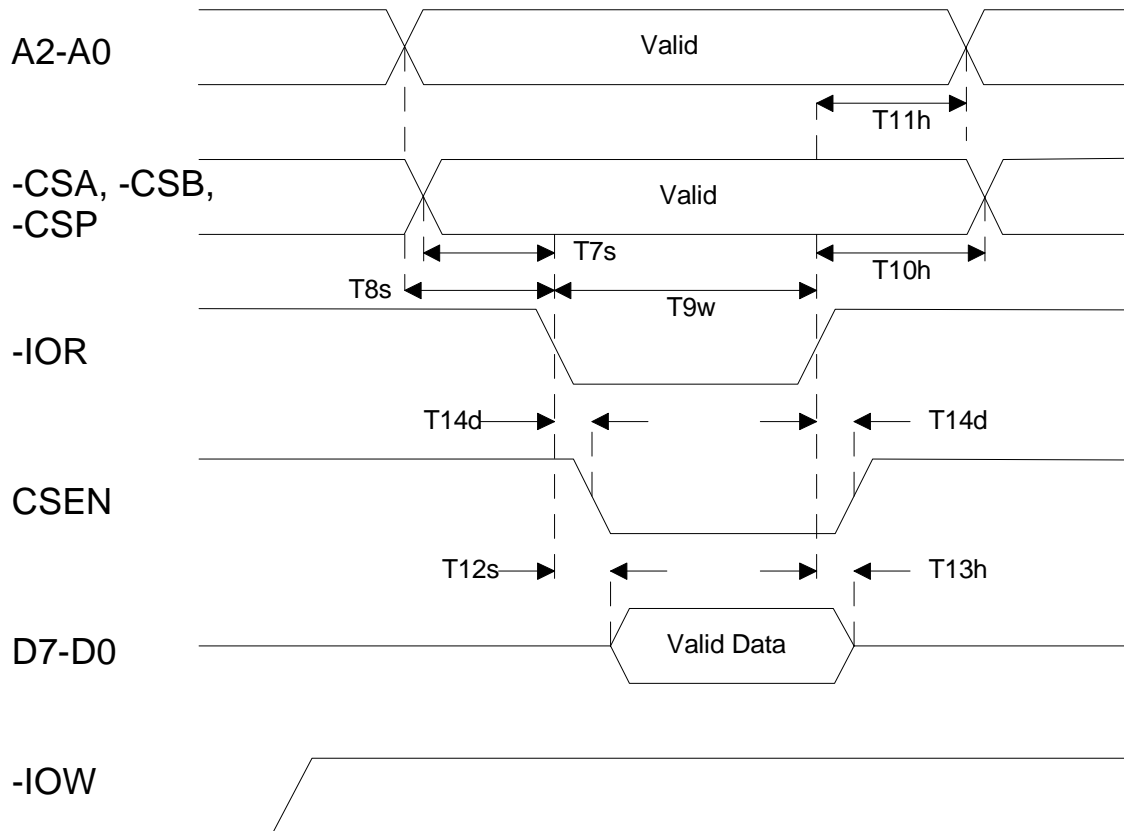
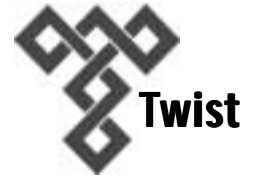
## AC Electrical Specifications

T = 0° C to 70° C (T = -40° C to +85° C for industrial tested "I" grade parts), VCC = 3.3V to 5V ± 10% unless otherwise specified.

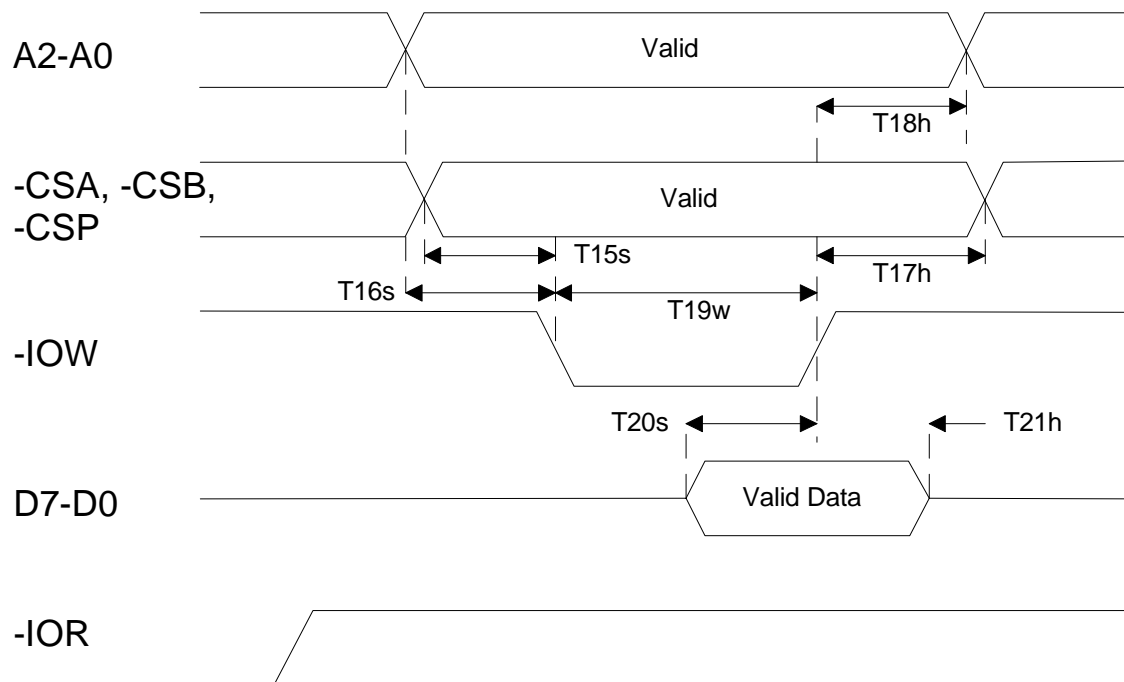
Symbol	Parameter	Limits 3.3V		Limits 5V		Unit	Condition
		Min	Max	Min	Max		
T1w	Reset strobe width	2500		2000		ns	
T5w	-CS A/B strobe width	60		50		ns	
T5s	Chip select setup time	8		5		ns	
T6h	Chip select hold time	0		0		ns	
T7s	-IOR setup time	8		5		ns	-AS=0
T9w	-IOR strobe width	40		35		ns	
T10h	-IOR hold time	15		10		ns	-AS=0
T12s	D0-D7 setup time	25		20		ns	
T13h	D0-D7 hold time		10		5	ns	
T14d	-IOR to -DDIS out		15		15	ns	
T15s	-IOW setup time	8		5		ns	-AS=0
T17h	-IOW hold time	15		10		ns	-AS=0
T19w	-IOW strobe width	40		35		ns	
T20s	D0-D7 setup time	20		15		ns	
T21h	D0-D7 hold time		10		5	ns	
T22d	Delay from THR write to -TXRDY high		40		35	ns	100 pf load
T23d	Delay from Start bit to -TXRDY low		8		8	Rclk	
T24d	Delay from Stop bit to set interrupt	8	9	8	9	Rclk	
T25d	Delay from RHR read to Reset interrupt		40		35	ns	100 pf load
T26d	Delay from Stop bit to set -RXRDY low		1		1	Rclk	
T27d	Delay from RHR trigger Level to -RXRDY low	8	9	8	9	Rclk	
T28d	Modem output delay		50		45	ns	
T29d	Delay from Modem input Change to interrupt		40		35	ns	100 pf load
T30d	Delay from MCR read to Clear interrupt		40		35	ns	100 pf load
T31w	Clock pulse duration	20		17		ns	
T32w	Clock pulse duration	20		17		ns	
T33	Clock frequency		16		24	MHz	
T34d	Delay from ACK to Interrupt		40		35	ns	
T35d	Delay from STR read to Clear interrupt		40		35	ns	

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Dual UART with 16-byte FIFO  
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**Figure 1. Read Cycle Timing Waveform**



**Figure 2. Write Cycle Timing Waveform**

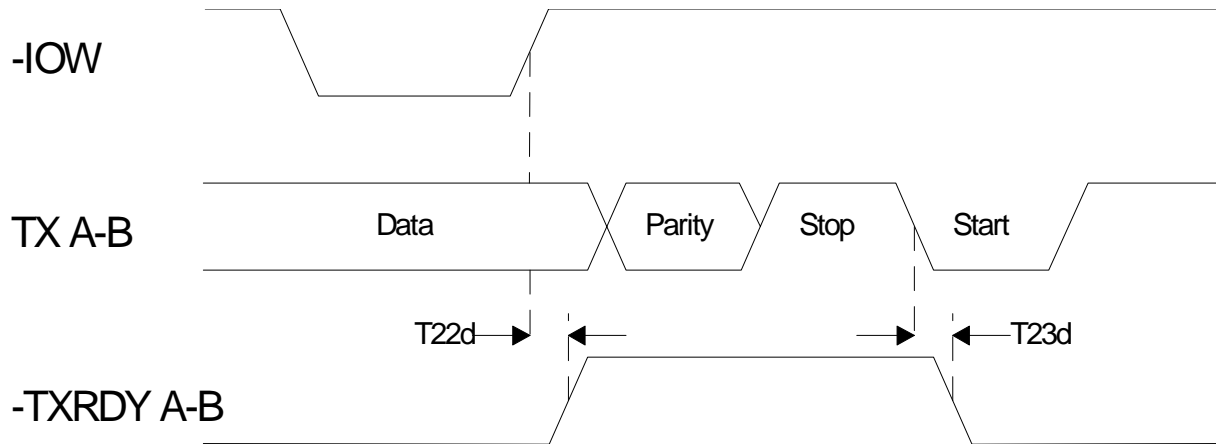


Figure 3. Transmitter Ready Mode "0" Timing Waveform

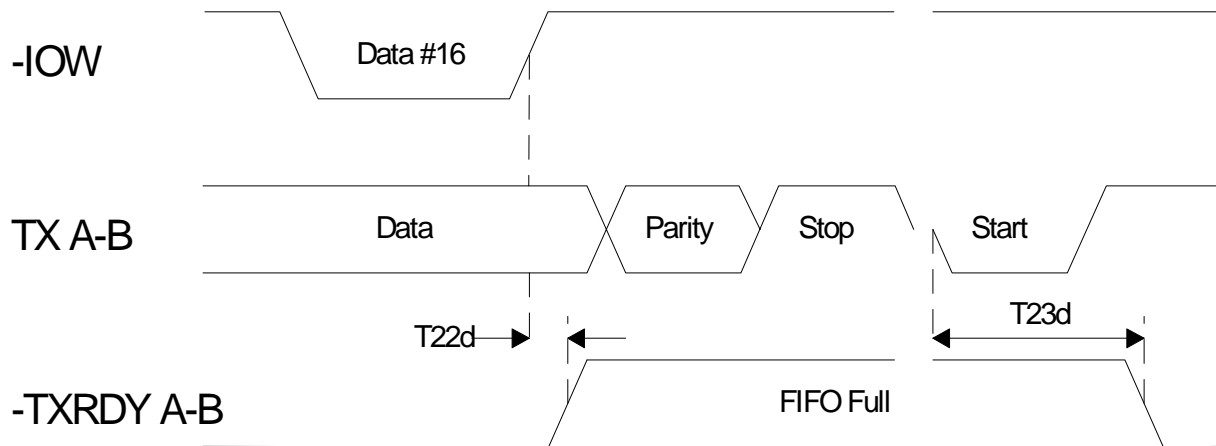


Figure 4. Transmitter Ready Mode "1" Timing Waveform

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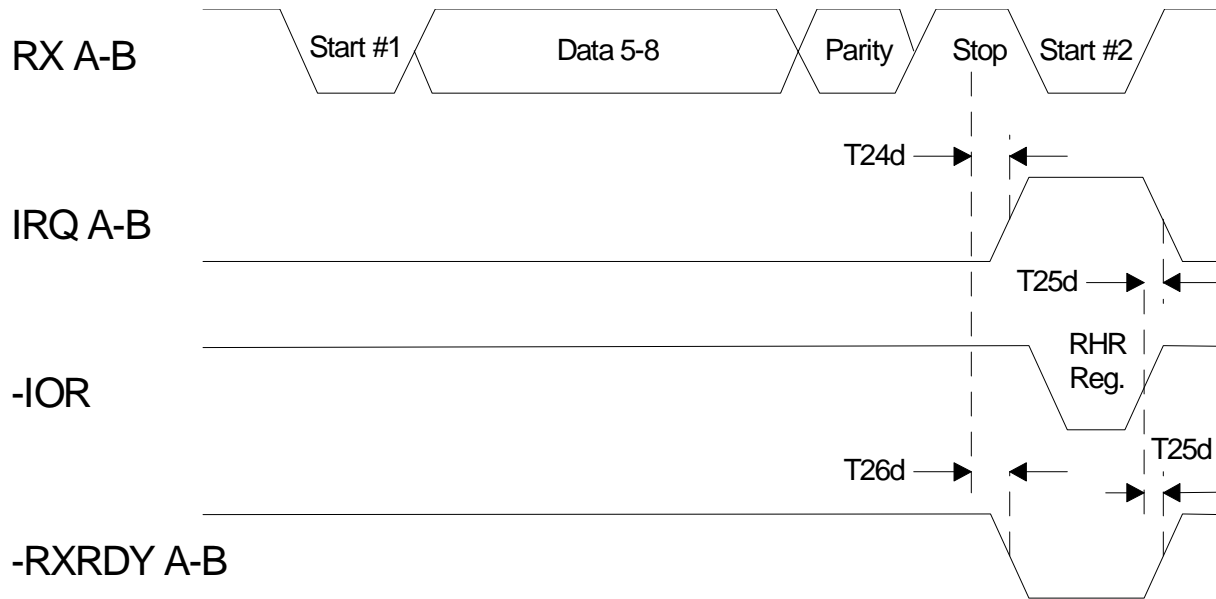


Figure 5. Receive Ready Mode "0" Timing Waveform

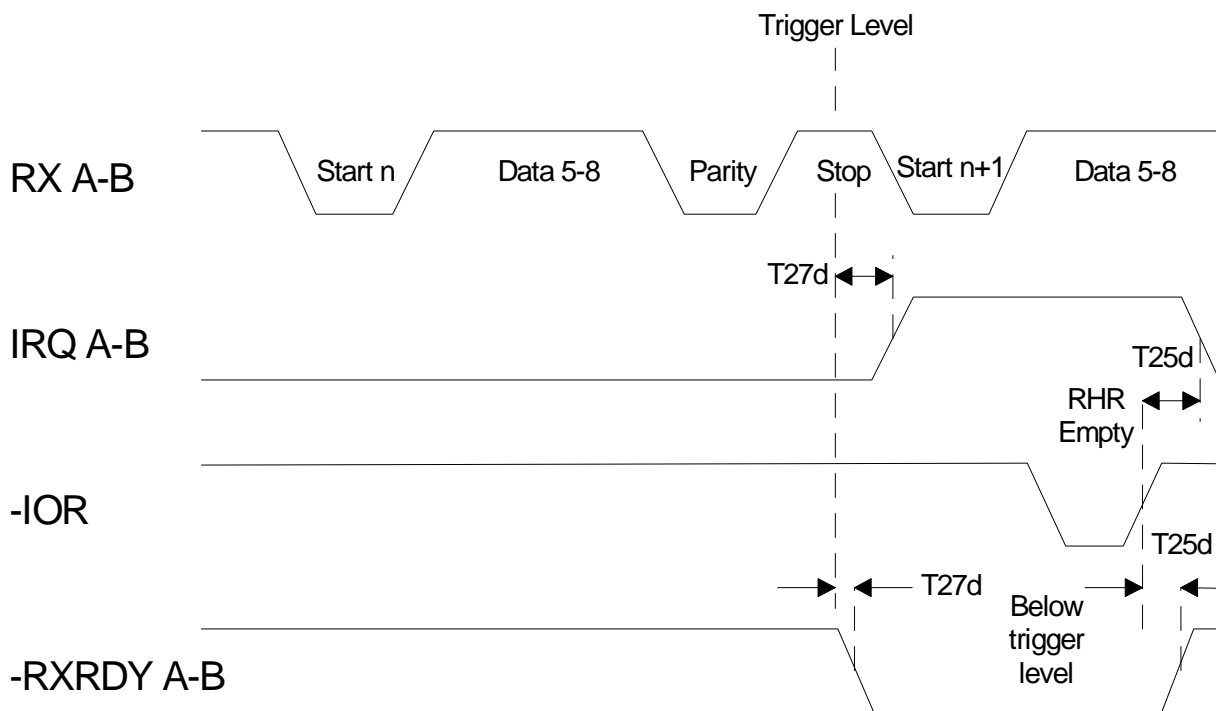


Figure 6. Receive Ready Mode "1" Timing Waveform



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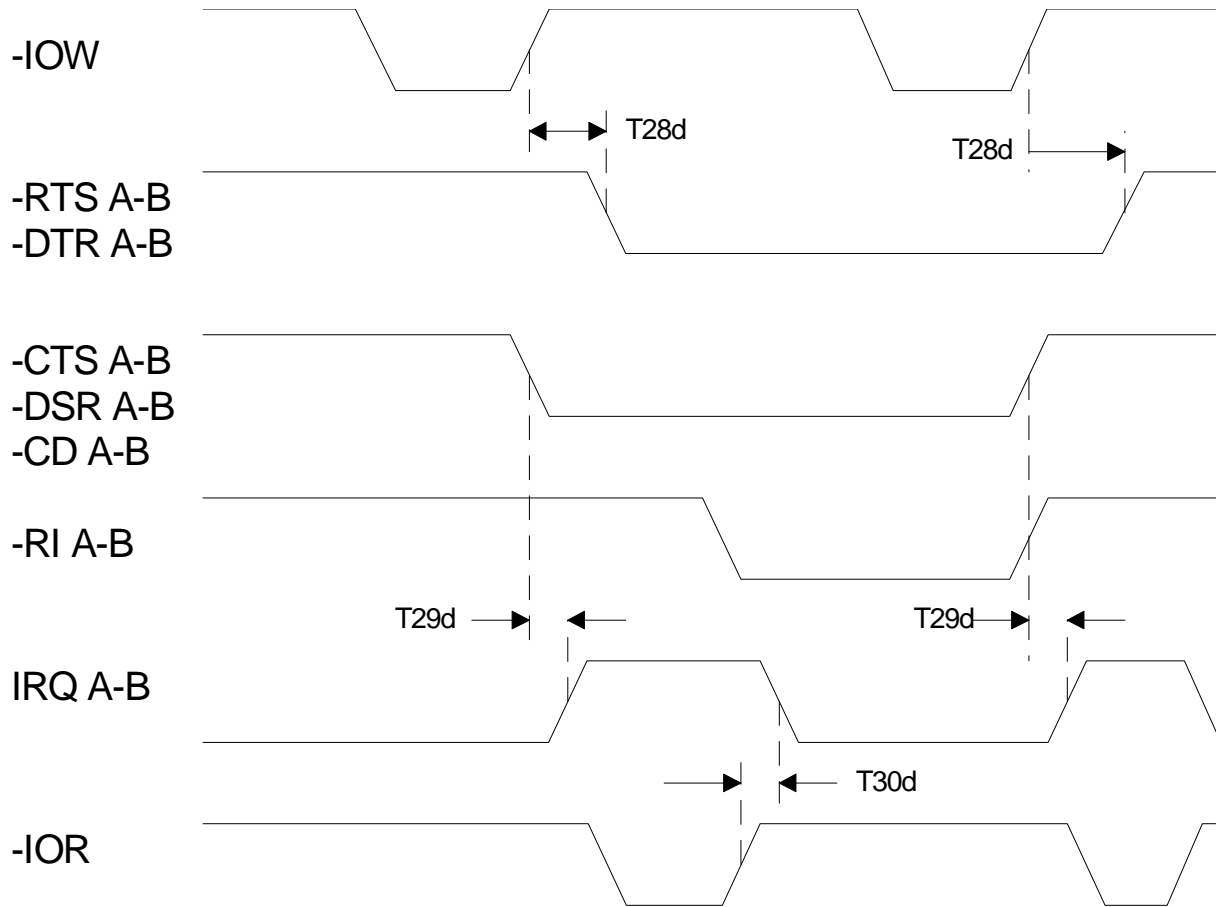


Figure 7. Modem Control Timing Waveform

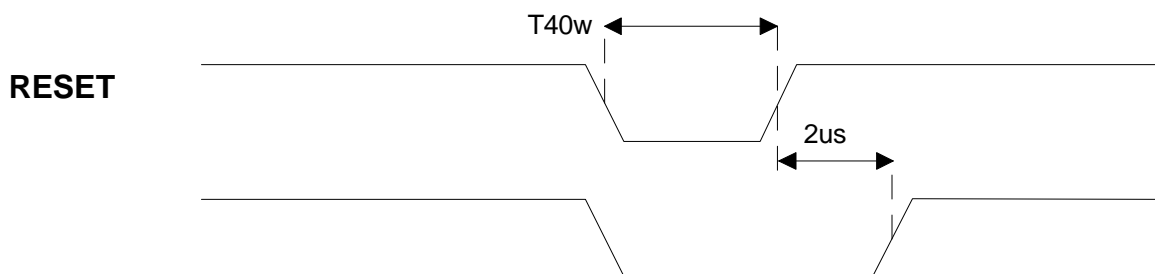


Figure 8. Power-On-Reset Timing Waveform

# TG16C552

Dual UART with 16-byte FIFO  
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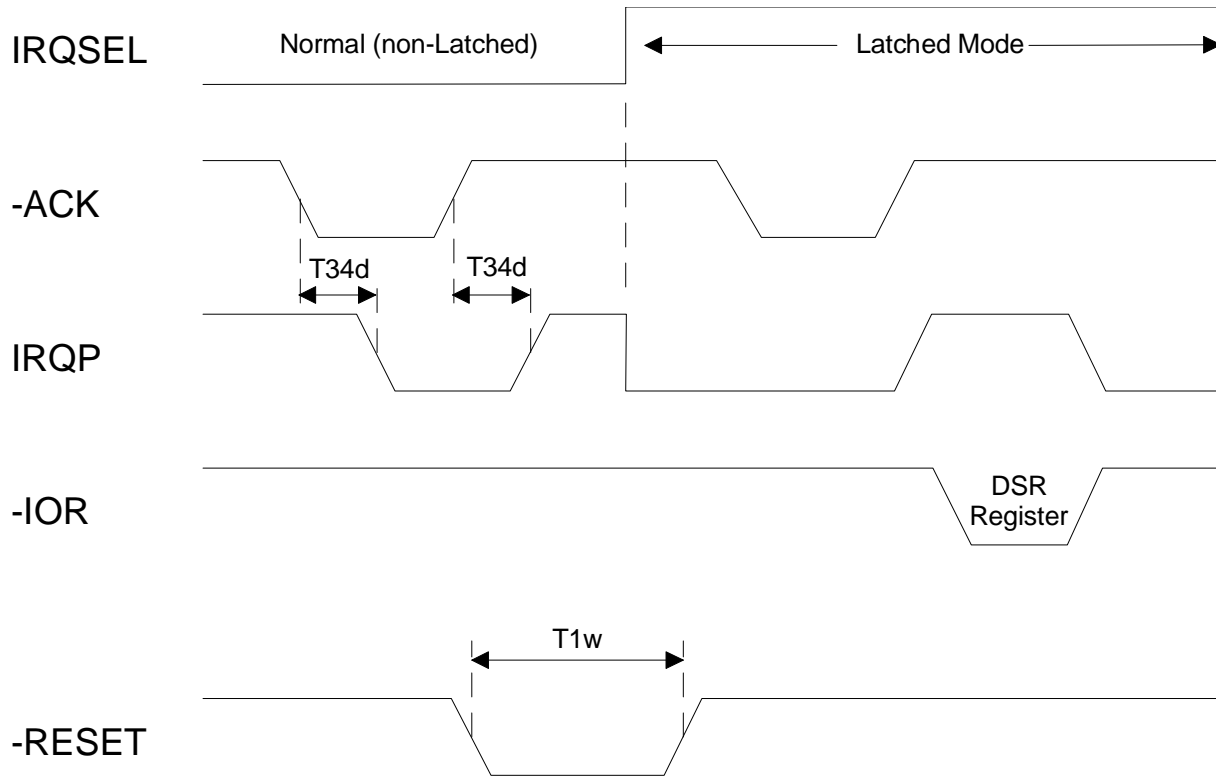


Figure 9. Printer Interrupt Timing Waveform

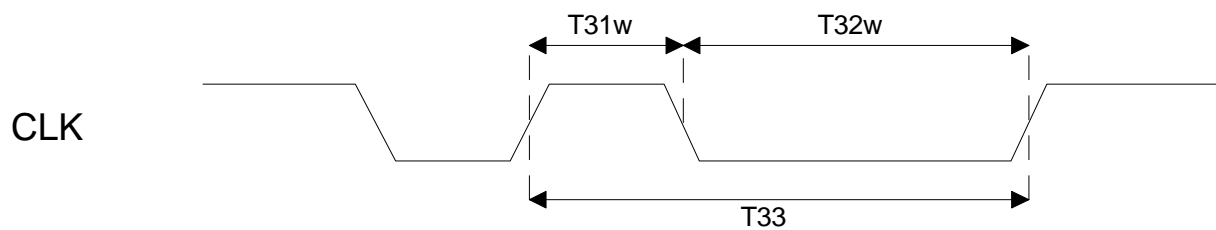


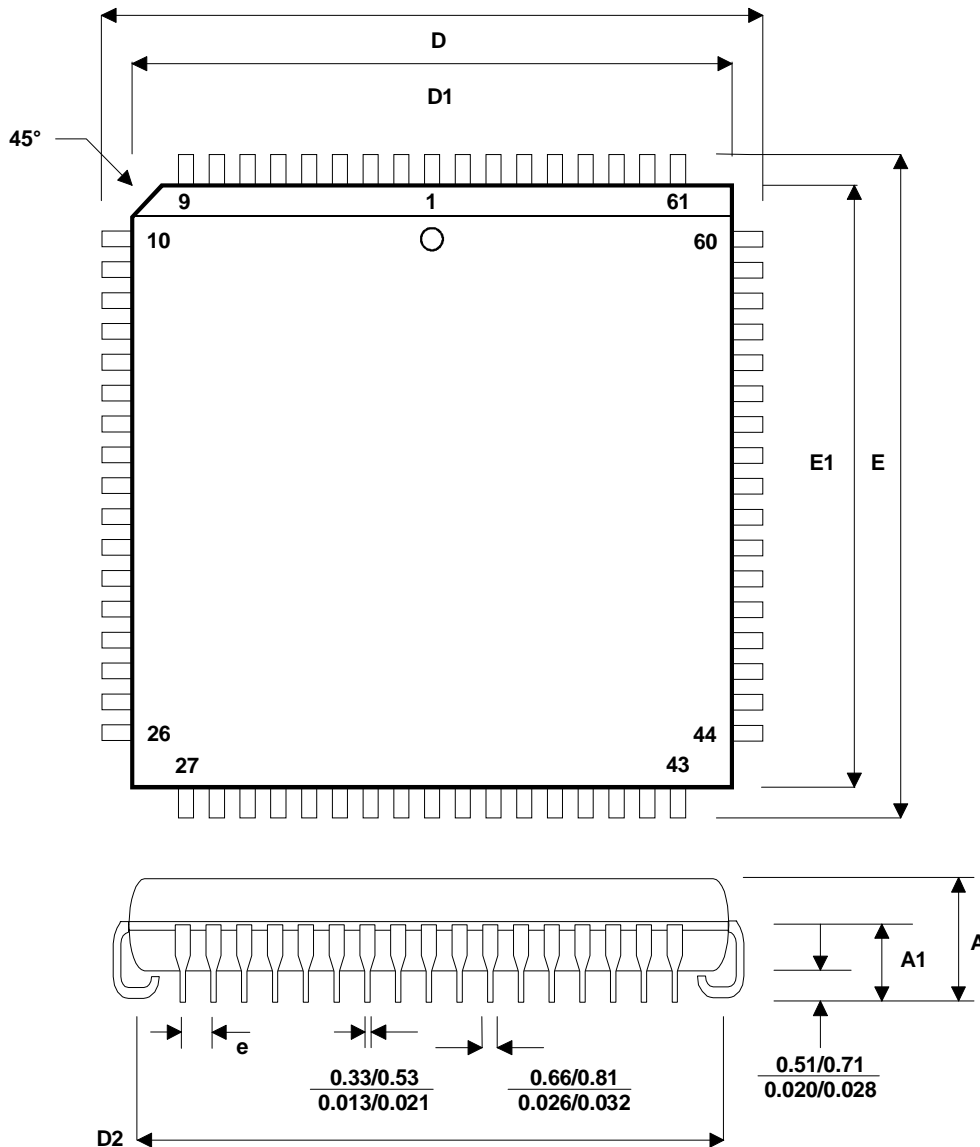
Figure 10. Clock Timing Waveform



# TG16C552

Dual UART with 16-Byte FIFO  
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## 68-Pin PLCC Package Outline



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.19	5.08	0.165	0.200
A1	2.29	3.30	0.090	0.130
e	1.27 TYP		0.050 TYP	
D/E	25.02	25.40	0.985	1.000
D1/E1	24.13	24.33	0.950	0.958
D2	22.40	23.82	0.882	0.948



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